Meet 1

Desing Philosophy -> Add details Verilog, Quartus, Model Sim, Reader is ignorant. Will we build an interpreter/assembler. Everything you have done, are going to be done.   
  
Register changes -. Organize Registers, Assembler Temporaries

Double Check Opcode

Make the change from SE + imm

Test all branches,   
  
May require more more branches

Jal Type – Change to push one IMM bit so that rd starts from uniformity.

Double Check bit shifting if its absolutely necessary.

Bit Shifts for branching

Interpret as Bytes

Memory Map {add stack}, {how many bytes}

Addressing Modes check commit?   
  
Calling convention on return value placements ->Add that in

Align Comments

Concise Tables

Talk about terminology.

How are we going to handle input output.